Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **NC**
2. **–IN**
3. **+IN**
4. **V- (-VS)**
5. **NC**
6. **OUT**
7. **V+ (+VS)**

**.031”**

**.036”**

**7 7 NC**

**6**

**4**

**2 3 4**

**MASK**

**REF**

**C8001**

**AD1**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: +VS**

**Mask Ref: C8001**

**APPROVED BY: DK DIE SIZE .031” X .036” DATE: 9/23/21**

**MFG: ANALOG DEVICES THICKNESS .008” P/N: AD8001A**

**DG 10.1.2**

#### Rev B, 7/19/02